EPTC 2020

22nd Electronics Packaging Technology Conference (Online)
2nd to 29th December 2020 , Singapore

IEEE EPS Flagship Conference
in Asia Pacific Region

1st Call for Registration and Participation

Dear Electronics Packaging Colleagues,

First and foremost, I hope that everyone is coping well despite the disruptions caused by the pandemic. We are all affected in one way or another, and it is more important than ever to support each other. We also quickly learned that digital transformation, which all of us have a key role to play, becomes more essential than before. Understanding what is at stake and to ensure continuity, the EPTC 2020 organising committee have decided to carry on with the cause.

The 22nd Electronics Packaging Technology Conference (EPTC 2020) is an international event organized by the IEEE RS/EPS/EDS Singapore Chapter and sponsored by IEEE Electronics Packaging Society (EPS). Since its inauguration in 1997, EPTC has developed into a highly reputed electronics packaging conference in the Asia-Pacific and is well attended by experts in all aspects of packaging technology from all over the world. EPTC is now the flagship conference of IEEE EPS in Region 10.

We appreciate your continued support despite the unusual time. EPTC 2020 will be run as a fully online event of **on-demand presentations (Dec 2 – 29, 2020)**, as well as **live presentations (Dec 2-3, 2020)**. The contents from the live presentations will be recorded and available on-demand post-event.

EPTC 2020 will feature Keynotes, Technology Talks, Panel Discussion, HIR Workshop, Forum, Invited Talks and Technical Sessions. We are very grateful to our sponsors who have continued to provide generous supports despite the uncertainties. These supports have enabled us to keep the registration fee affordable. We only ask for a **nominal fee of S$30** for you to access all the online contents (on-demand and live). In addition, a copy of the conference proceedings can be downloaded for S$50 only.

EPTC 2020 **Registration fee** can be found here

EPTC 2020 **Registration** can be completed here

EPTC 2020 **Advance program** can be found here

Let me walk you through the digital platforms we use to run EPTC 2020. Registration can be completed via **ConfTool** (https://www.conftool.org/eptc2020/). The online contents will be delivered and hosted via **Whova** (https://whova.com/portal/webapp/virtu2_202012/). Upon successful registration, you will receive the instructions to set up your login a few days closer to the actual conference dates. The Whova platform allows you to view the contents from the comfort of your desktop/laptop or mobile devices, any where any time.

The Program highlights are as follows:

KEYNOTES

KEYNOTE I
TBC
MANISH RANJAN
MANAGING DIRECTOR - DEPOSITION PRODUCT GROUP
LAM RESEARCH

KEYNOTE II
HETEROGENEOUS INTEGRATION FOR HPC APPLICATIONS DRIVEN BY 5G AND AI
JOHN H LAU
CTO
UNIMICRON TECHNOLOGY CORPORATION

TECHNOLOGY TALKS

TECHNOLOGY TALK I
THE PROMISE OF ADVANCED PACKAGING FOR MOORE'S LAW
RAMESH CHIDAMBARAM
STRATEGIC MARKETING DIRECTOR
APPLIED MATERIALS

TECHNOLOGY TALK II
HETEROGENOUS WAFER LEVEL 2.5D AND 3D INTEGRATION
SEUNG WOOK YOON
CORPORATE VP / PACKAGE TECHNOLOGY PLANNING, TEST & SYSTEM PACKAGE
SAMSUNG ELECTRONICS CORPORATION

PANEL

"PANEL LEVEL PACKAGING"

Panel Level Packaging is the latest trend in microelectronics packaging. This method has the potential to offer significant package miniaturization (volume and thickness), high throughout manufacturing and lower cost of ownership. It also improves the electrical and thermal performance, enabling a range of applications in heterogeneous integration. In this panel discussion, experts will share theirs experiences and views on this promising technology covering technology options, challenges and solutions, use cases and the future outlook.

The Panel will be moderated by Sam Karikalan (Broadcom) and the speakers include Tanja Braun (Fraunhofer IZM), Rozalia Beica (AT&S), C. P. Hung (ASE), Tim Olson (Deca) and Tingyu Lin (NCAP).

WORKSHOP

"Heterogeneous Integration Roadmap (HIR)"

The Heterogeneous Integration Roadmap (HIR), released October 2019, is a roadmap to the future of electronics identifying technology requirements and potential solutions. The primary objective is to stimulate pre-competitive collaboration between industry, academia and government to accelerate progress. The roadmap offers professionals,

industry, academia and research institutes a comprehensive, strategic forecast of technology over the next 15 years. The HIR also delivers a 25-year projection for heterogeneous integration of Emerging Research Devices and Emerging Research Materials with longer research-and-development timelines.

The HIR Workshop at EPTC 2020 features overall updates on the HIR (Bill Chen, ASE), updates on selected chapters on 2.5D/3D (Ravi Mahajan, Intel) Photonics Technology (Bill Bottoms, Third Millenium Test Solutions), Data Center/HPC (Kanad Ghose, Binghamton University) and Security (Sohrab Aftabjahani, Intel). There will be a live panel on Photonics Technology moderated by Surya Bhattacharya, Director of Systems in Package at the Institute of Microelectronics, Singapore, and co-moderated by C. P. Hung, Vice President, Corporate R&D of ASE Group.

FORUM

"Advanced Packaging for Mobile Applications"

Details to be finalized

INVITED PRESENTATIONS

There are **12 invited presentations** by experts from industry and academia on emerging topics in electronics packaging. The industry experts are from Applied Materials, ASM, GlobalFoundries, Samsung, Zeiss, SPIL, JCET, Inphi and Yole. We also have invited talks from distinguished professors from Purdue University, Portland State University, and Lamar University.

CONFERENCE TOPICS

There are all together **102 technical presentations** covering important aspects of electronics packaging as listed below.

- 2.5D, 3D and TSV Processes
- Advanced FA and Reliability
- Advanced Flip Chip, Substrate and SiP
- Advanced Materials and Processing
- Advanced Package Designs and Characterization
- Assembly and Manufacturing Technology
- Emerging Materials and Processing
- Flex and Printed Electronics
- Metrology and Inspection for Advanced Packaging
- RF, 5G and mmWave Packaging
- Silicon and Glass Interposer
- Solder Joint Characterization and Reliability
- Thermal Characterization and Cooling Solutions
- Thermo-Mechanical Simulation
- Wafer and Panel Level Processing
- Wafer Fab Out Processes
- Wafer Hybrid Bonding

We are particularly grateful for the continued and strong supports from our sponsors. Your supports have enabled us to carry on with the cause to provide a platform for timely dissemination of the latest technical knowledge to the electronics packaging community.

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HUAWEI

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APPLIED MATERIALS

ASE GROUP

Silver Sponsors

LINTEC
Linking your dreams

ZYMET

PacTech
member of nagase group

Bronze Sponsor

ZYMET

Best Student Paper Award

ASE GROUP

I recognise that EPTC 2020 is unlike the previous ones and we are humbled by your continued supports. It is my hope that you find this EPTC 2020 online experience an enriching one. I am sure we will emerge stronger from this pandemic and I hope to be able to meet everyone in-person in 2021.

Most sincerely,

Chuan Seng Tan
Nanyang Technological University, Singapore

General Chair
https://www.eptc-ieee.net